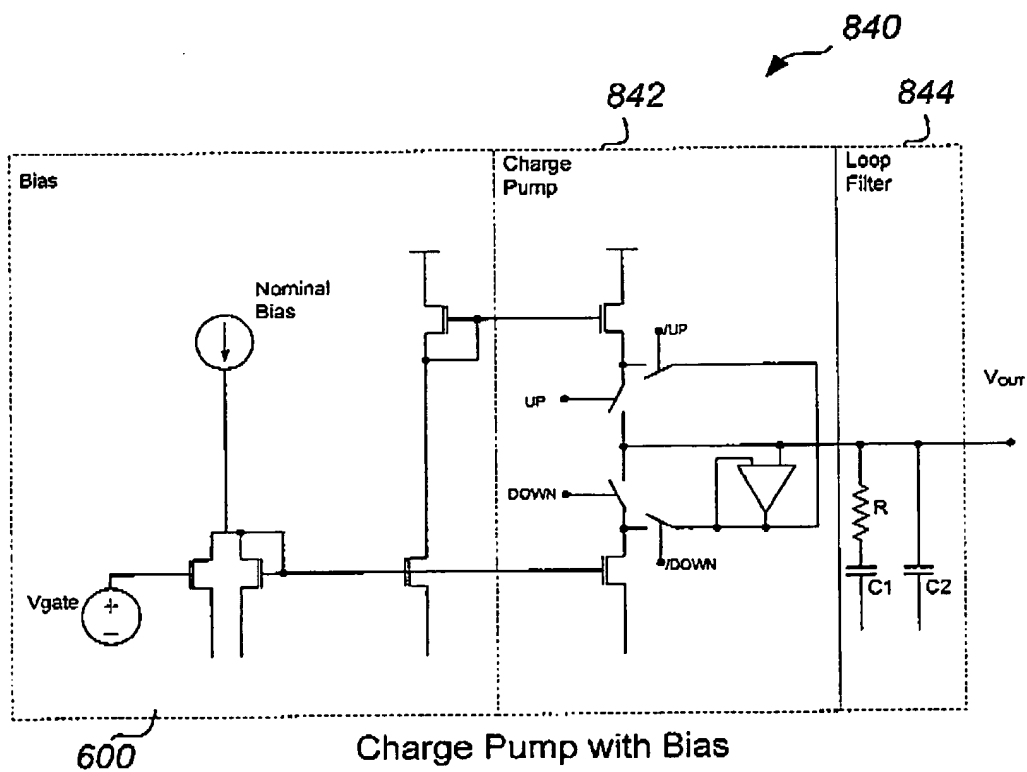
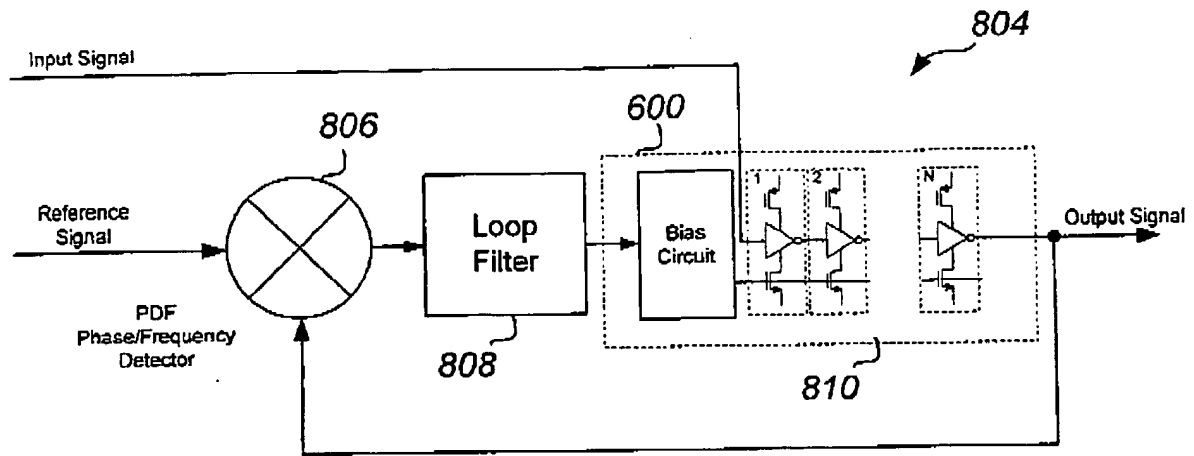
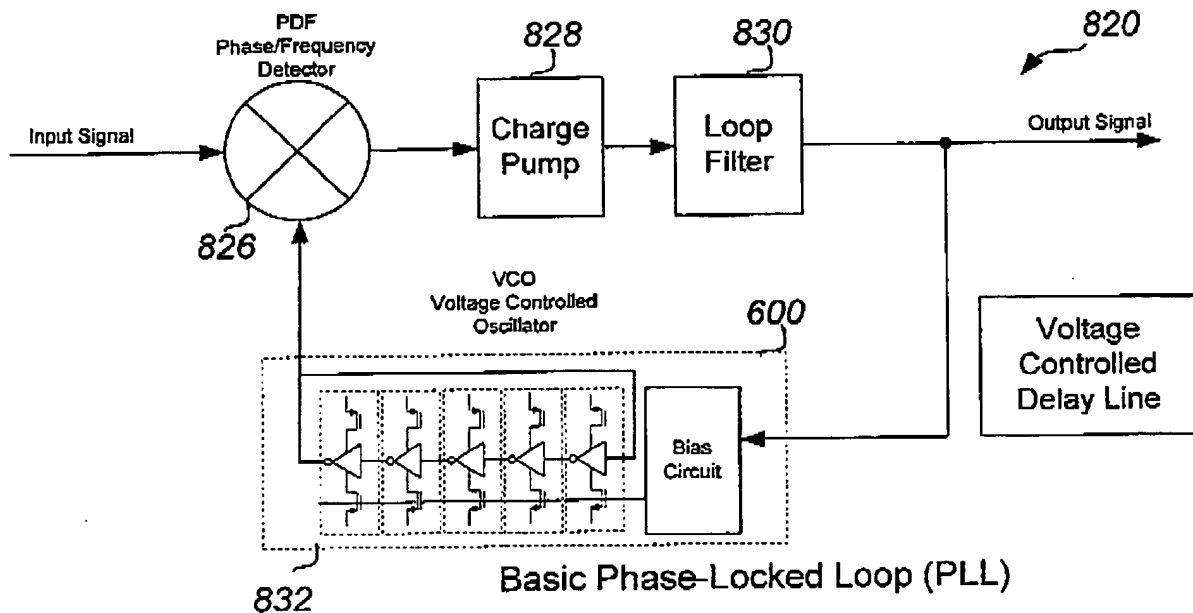
**Fig. 19****Fig. 22**

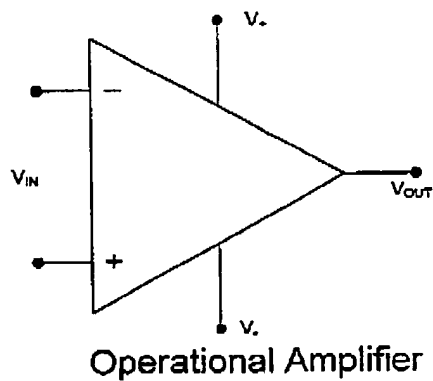
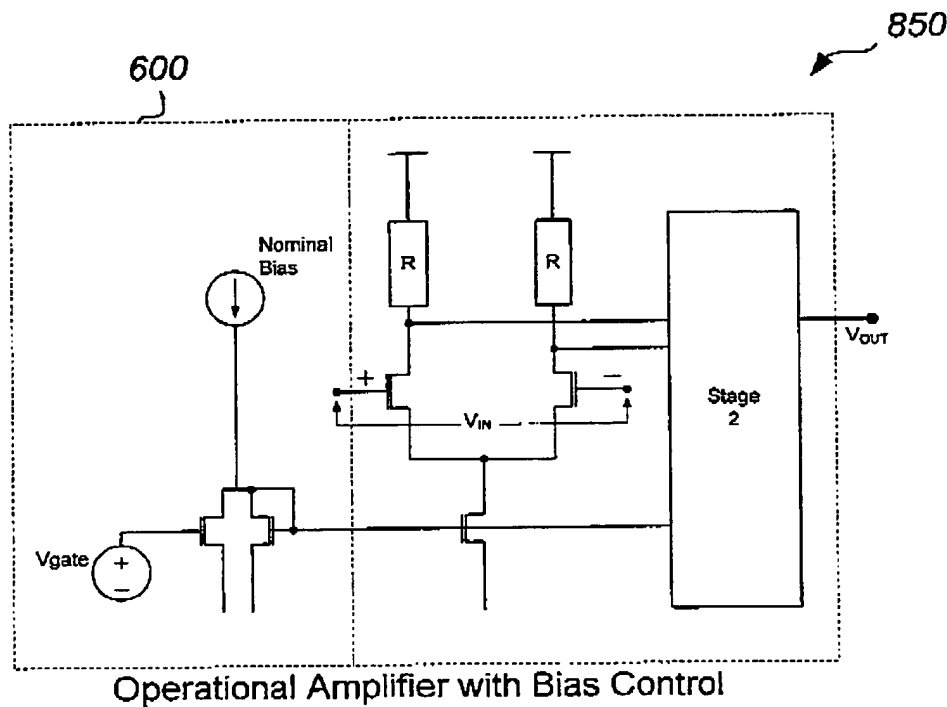


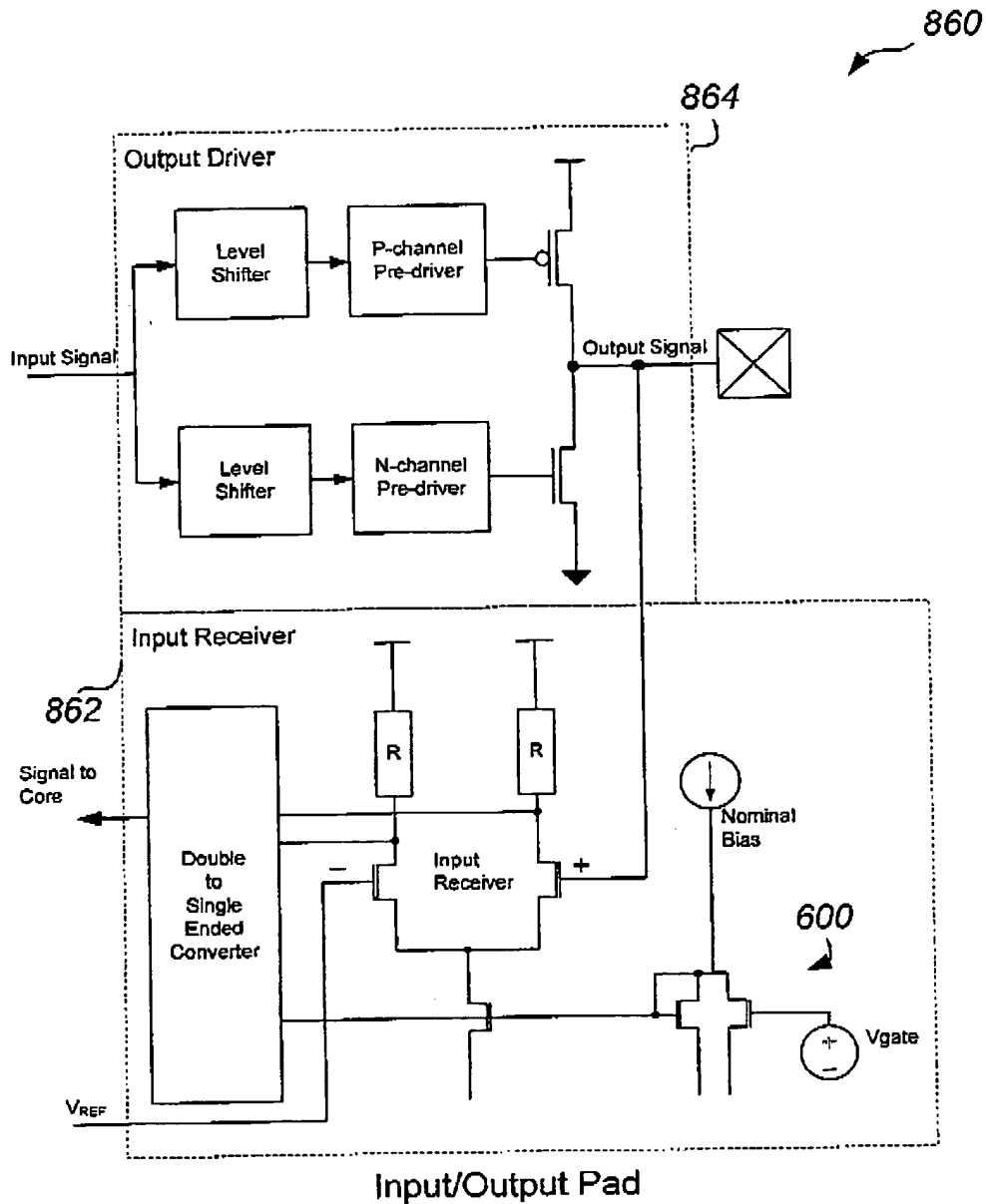
Basic Delay-Locked Loop (DLL)

**Fig. 20**

Basic Phase-Locked Loop (PLL)

**Fig. 21**

**Fig. 23a****Operational Amplifier with Bias Control****Fig. 23b**



**Fig. 24**